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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,658	12/05/2005	Yasushi Takahashi	1374.45607X00	7191

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EXAMINER	
PHAM, LONG	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
03/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/559,658	TAKAHASHI, YASUSHI	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *4-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/05/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1, 2, and 3 in the reply filed on 01/05/09 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kenji (Japan 04039959).

With respect to claim 1, Kenji teaches a semiconductor device, comprising (see figs. 1-4 and associated text):

a semiconductor chip 1 which has a main surface and a back surface which are mutually located in an opposite side, and a plurality of electrode pads arranged over the main surface;

a capacitative element 2 which has a first and a second electrode;

a supporting body 3 which has a main surface and a back surface which are mutually located in an opposite side;

a plurality of leads 6,8,9,10, etc arranged around the supporting body;

a plurality of bonding wires which connect electrically the electrode pads of the semiconductor chip, and the leads; and

a resin sealing body 5 which seals the semiconductor chip, the capacitative element, the supporting body, the leads, and the bonding wires;

wherein

the leads extend and exist continuing in and out of the resin sealing body;

the semiconductor chip is adhered over the main surface of the supporting body; and

the capacitative element is adhered over the back surface of the supporting body.

Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Kenji (Japan 04039959).

With respect to claim 2, Kenji teaches a semiconductor device, comprising (see figs. 1-4 and associated text):

a semiconductor chip 1 which has a main surface and a back surface which are mutually located in an opposite side, and a controlling circuit and a plurality of electrode pads which have been arranged in the main surface;

a capacitative element 2 which has a first and a second electrode;

a first supporting body 3 that has a main surface and a back surface which are mutually located in an opposite side;

a second supporting body (left and right portion of 3) that is the second supporting body arranged around the first supporting body, and has a main surface and a back surface which are mutually located in an opposite side, and with which the main surface is located in a same side as the main surface of the first supporting body in a thickness direction of the first supporting body;

a plurality of leads 6,8,9,10, etc arranged around the first supporting body;

a plurality of bonding wires which connect electrically the electrode pads of the semiconductor chip, and the leads, and the main surface of the second supporting body; and

a resin sealing body 5 which seals the semiconductor chip, the capacitative element, the first and the second supporting body, the leads, and the bonding wires;

wherein the leads extend and exist continuing in and out of the resin sealing body;

the semiconductor chip is adhered over the main surface of the first supporting body;

the first electrode of the capacitative element is adhered over the back surface of the first supporting body; and

the second electrode of the capacitative element is adhered over the back surface of the second supporting body.

Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Kenji (Japan 04039959).

With respect to claim 3, Kenji teaches a semiconductor device, comprising (see figs. 1-4 and associated text):

a semiconductor chip which has a main surface and a back surface which are mutually located in an opposite side, and a controlling circuit and a plurality of electrode pads which have been arranged in the main surface;

a capacitative element which has a first and a second electrode;

a first supporting body that has a main surface and a back surface which are mutually located in an opposite side;

a second supporting body that is the second supporting body arranged around the first supporting body, and has a main surface and a back surface which are mutually located in an opposite side and with which the main surface is located in a same side as the main surface of the first supporting body in a thickness direction of the first supporting body;

a wire connecting part which is arranged around the first supporting body and connects with the first supporting body;

a plurality of leads 6, 8, 9, 10, etc arranged around the first supporting body;

a plurality of bonding wires which connect electrically the electrode pads of the semiconductor chip, and the leads, the wire connecting part and the main surface of the second supporting body; and

a resin sealing body 5 which seals the semiconductor chip, the capacitative element, the first and the second supporting body, the wire connecting part, the leads, and the bonding wires;

wherein the leads extend and exist continuing in and out of the resin sealing body;

the semiconductor chip is adhered over the main surface of the first supporting body;

the first electrode of the capacitative element is adhered over the back surface of the first supporting body; and

the second electrode of the capacitative element is adhered over the back surface of the second supporting body.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/Long Pham/
Primary Examiner, Art Unit 2814